WHAT IS CLAIMED IS:

1. A method for verifying a design of a circuit, comprising:

providing a model of the design;

providing a first property for the design, wherein the first property describes a first behavior;

checking the model using the first property and an environment of the design starting at a reset state until an example of the first behavior occurs;

providing a second property for the design, wherein the second property describes a second behavior; and

checking the model using the second property and an environment of the design starting at a state when the example of the first behavior occurs.

2. The method of claim 1, wherein providing the first property comprises:

providing a statement in a specification language stating that the first behavior does not occur.

3. The method of claim 2, wherein the environment of the design comprises one or more environment variables, and wherein checking the model using the first property comprises:

determining a set of values for the environment variables that causes the model of the design to show an example of the first behavior.

4. The method of claim 1, further comprising:

providing a state of the model of the design when the example of the first behavior occurs.

5. The method of claim 1, further comprising:

providing the environment of the design starting at the reset state.

6. The method of claim 1, further comprising:

providing the environment of the design starting at a state when the example of the first behavior occurs.

7. The method of claim 6:

wherein the environment of the design comprises one or more environment variables;

wherein the model of the design comprises one or more model variables; and

wherein providing the environment of the design starting at the state when the example of the first behavior occurs comprises at least one of the group consisting of:

describing the state when the example of the first behavior occurs; and

providing the values of the environment variables and the model variables in each clock cycle preceding the example when the first behavior occurs.

8. A computer program for verifying a design of a circuit, comprising:

providing a model of the design;

providing a first property for the design, wherein the first property describes a first behavior;

checking the model using the first property and an environment of the design starting at a reset state until an example of the first behavior occurs;

providing a second property for the design, wherein the second property describes a second behavior; and

checking the model using the second property and an environment of the design starting at a state when the example of the first behavior occurs.

9. The computer program of claim 8, wherein providing the first property comprises:

providing a statement in a specification language stating that the first behavior does not occur.

10. The computer program of claim 9, wherein the environment of the design comprises one or more environment variables, and wherein checking the model using the first property comprises:

determining a set of values for the environment variables that causes the model of the design to show an example of the first behavior.

11. The computer program of claim 8, further comprising:

providing a state of the model of the design when the example of the first behavior occurs.

12. The computer program of claim 8, further comprising:

providing the environment of the design starting at the reset state.

13. The computer program of claim 8, further comprising:

providing the environment of the design starting at a state when the example of the first behavior occurs.

14. The computer program of claim 13:

wherein the environment of the design comprises one or more environment variables;

wherein the model of the design comprises one or more model variables; and

wherein providing the environment of the design at the state when the example of the first behavior occurs comprises at least one of the group consisting of:

describing the state when the example of the first behavior occurs; and

providing the values of the environment variables and the model variables in each clock cycle preceding the example when the first behaviour occurs.